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Divan

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(54) **ACTIVE CURRENT SURGE LIMITERS WITH DISTURBANCE SENSOR AND MULTISTAGE CURRENT LIMITING**

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(60) Provisional application No. 60/648,466, filed on Jan. 31, 2005.

(51) **Int. Cl.**
H02H 9/08 (2006.01)

(52) **U.S. Cl.**
USPC **361/58**; 361/93.9

(58) **Field of Classification Search**
USPC 361/58, 93.9
See application file for complete search history.

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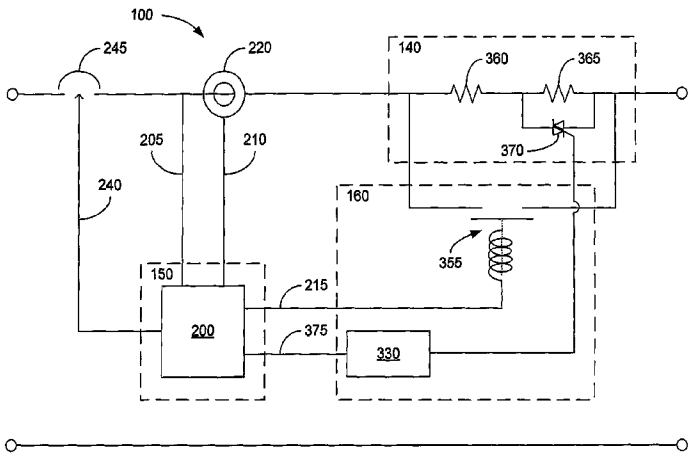
(57) **ABSTRACT**

Active current surge limiters and methods of use are disclosed. One exemplary system, among others, comprises a current limiter, including an interface configured to be connected between a power supply and a load; a disturbance sensor, configured to monitor the power supply for a disturbance during operation of the load; and an activator, configured to receive a control signal from the disturbance sensor and to activate the current limiter based on the control signal.

57 Claims, 6 Drawing Sheets



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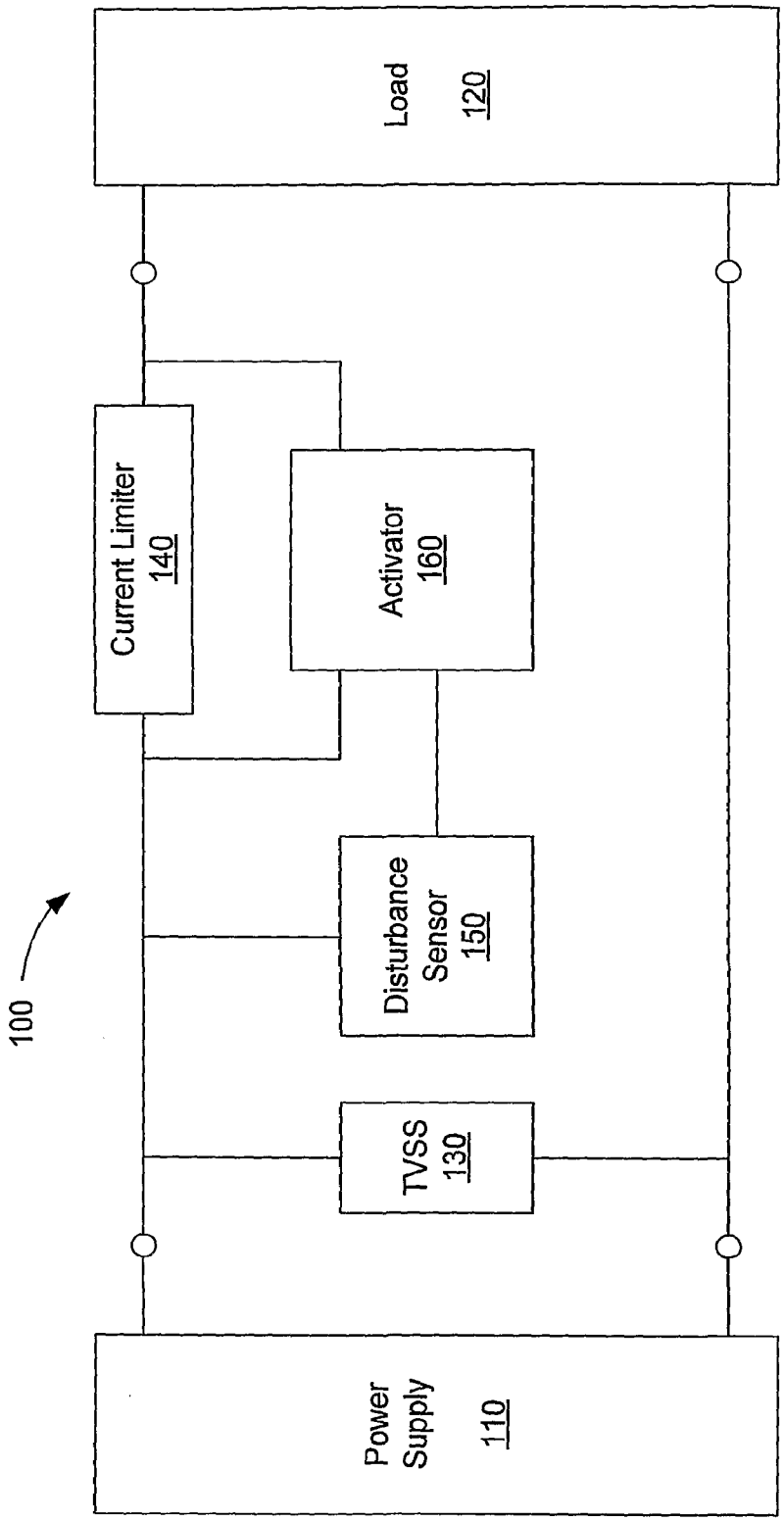
Load
120
Current Limiter
140
Activator
160
Disturbance
Sensor
150
TVSS
130
Power
Supply
110
100

FIG. 1

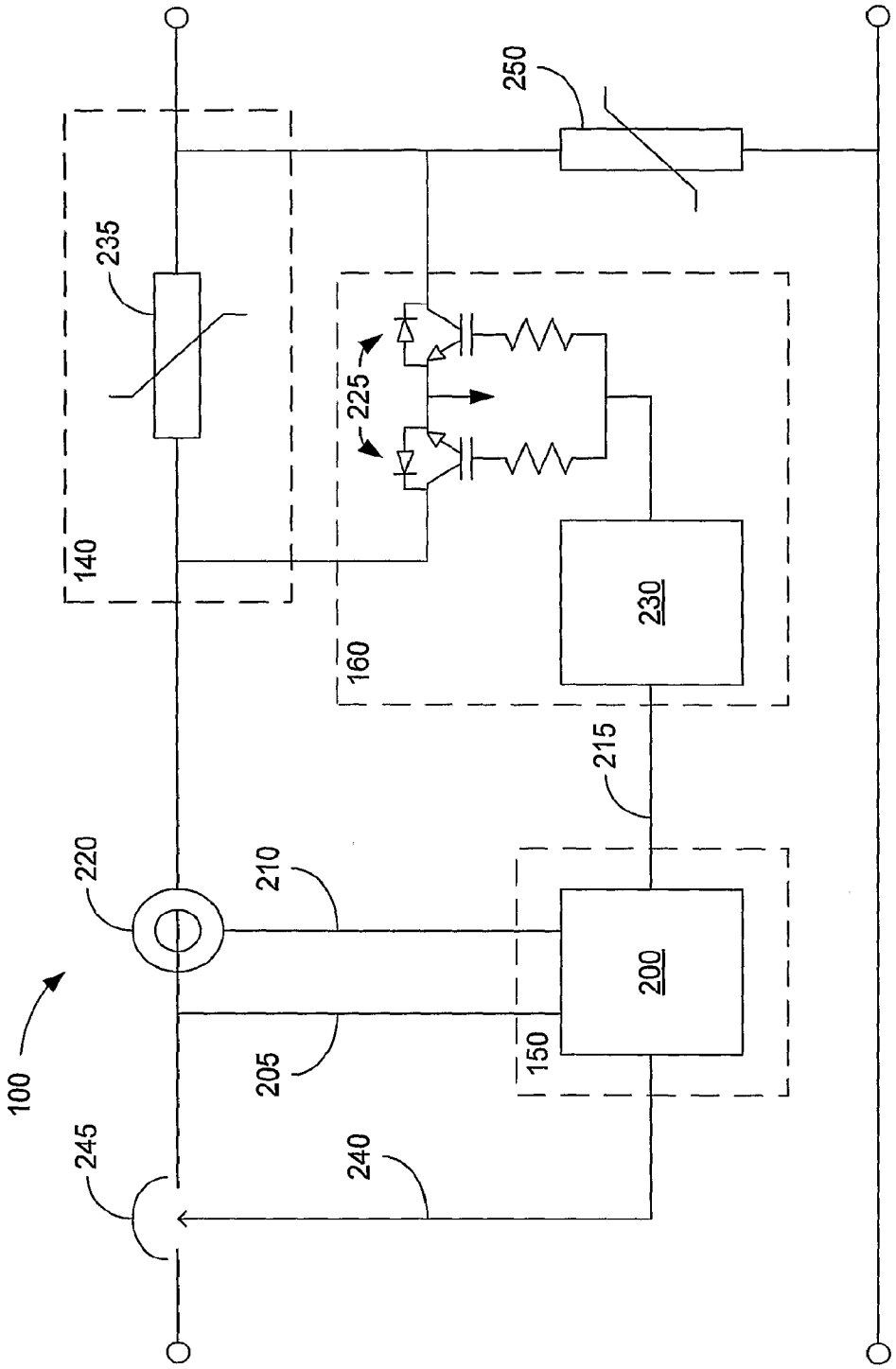

FIG. 2

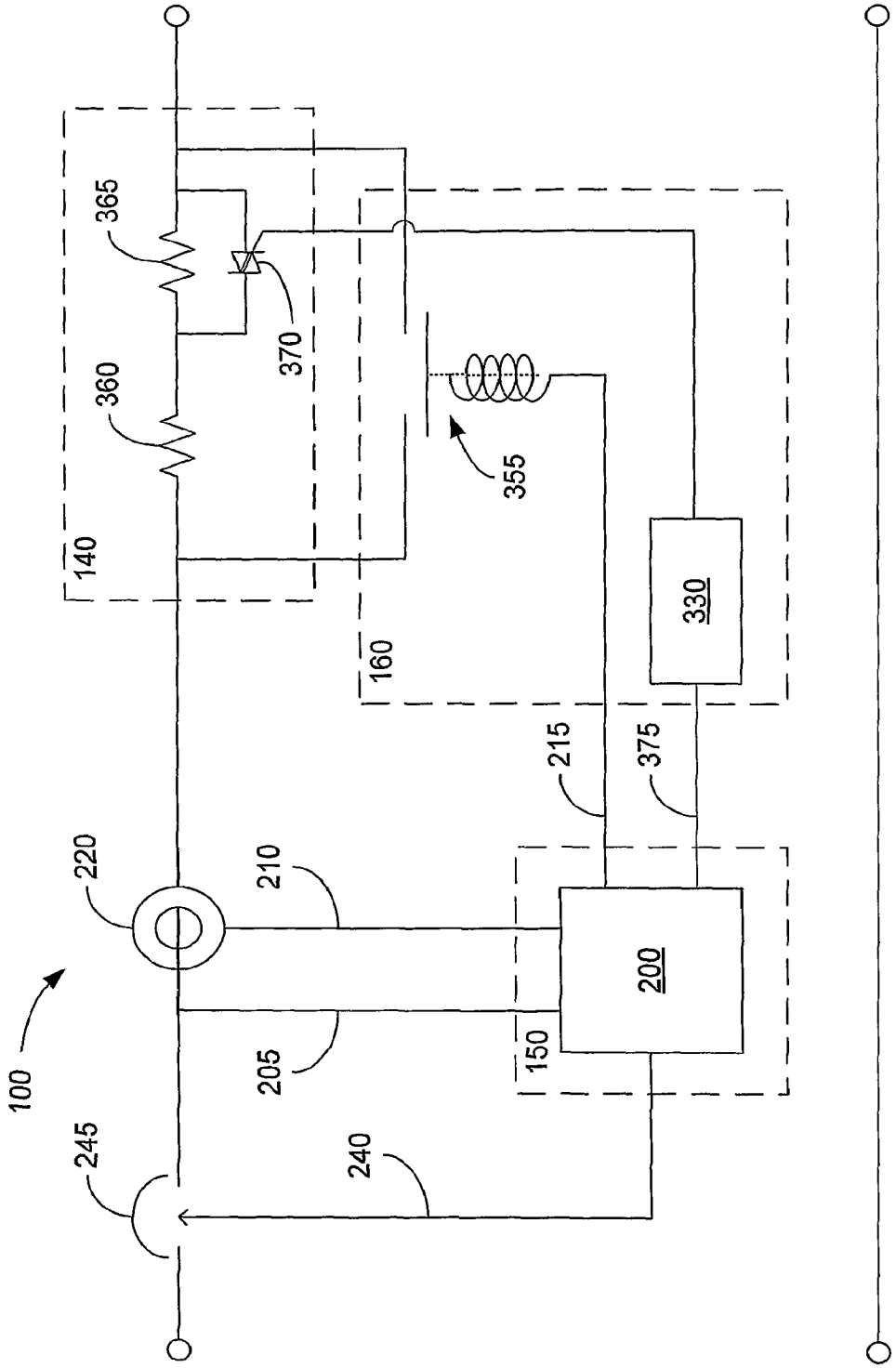
365
370
360
355
140
160
330
215
375
220
210
200
205
150
100
245
240

FIG. 3

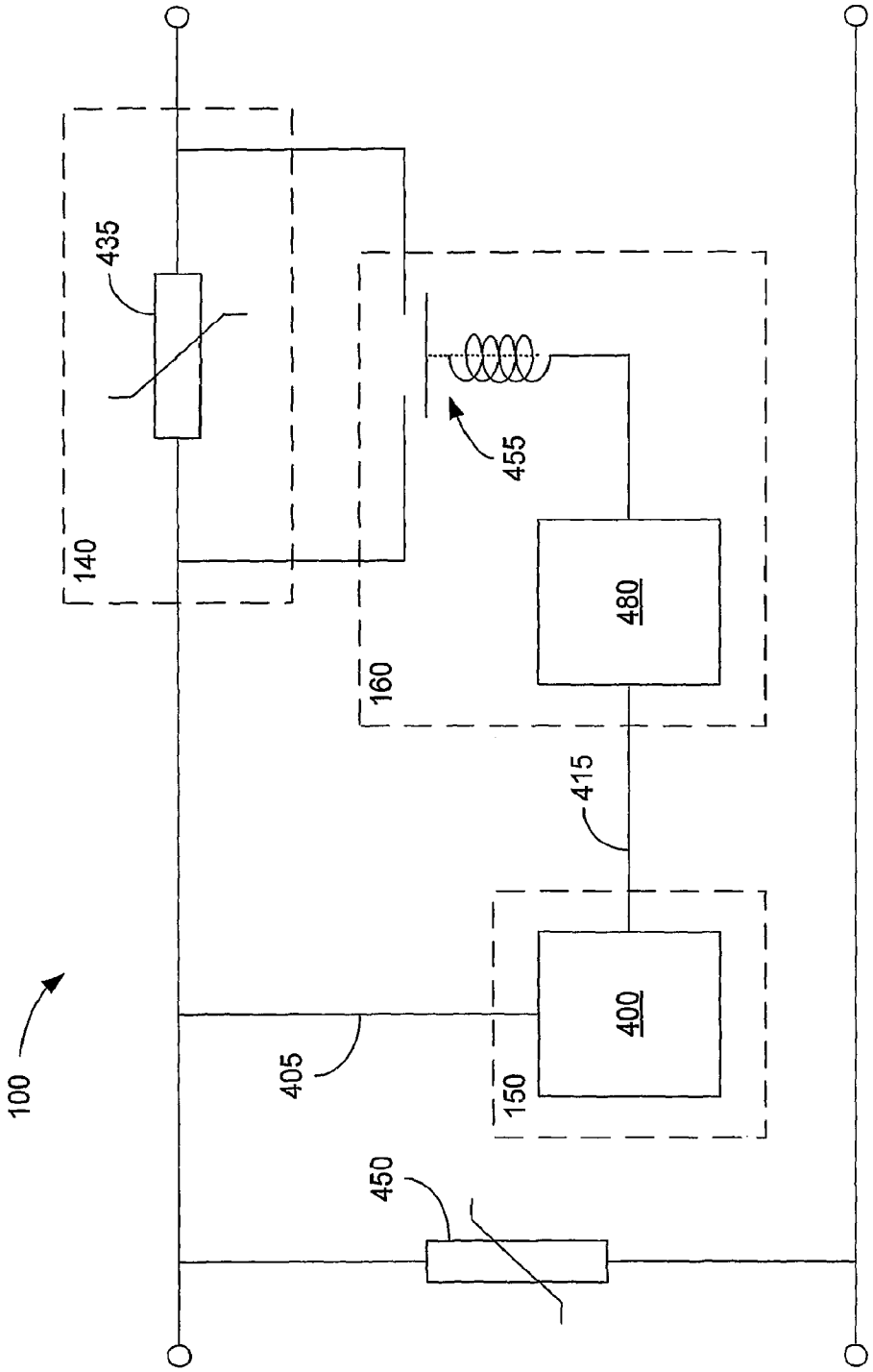

FIG. 4

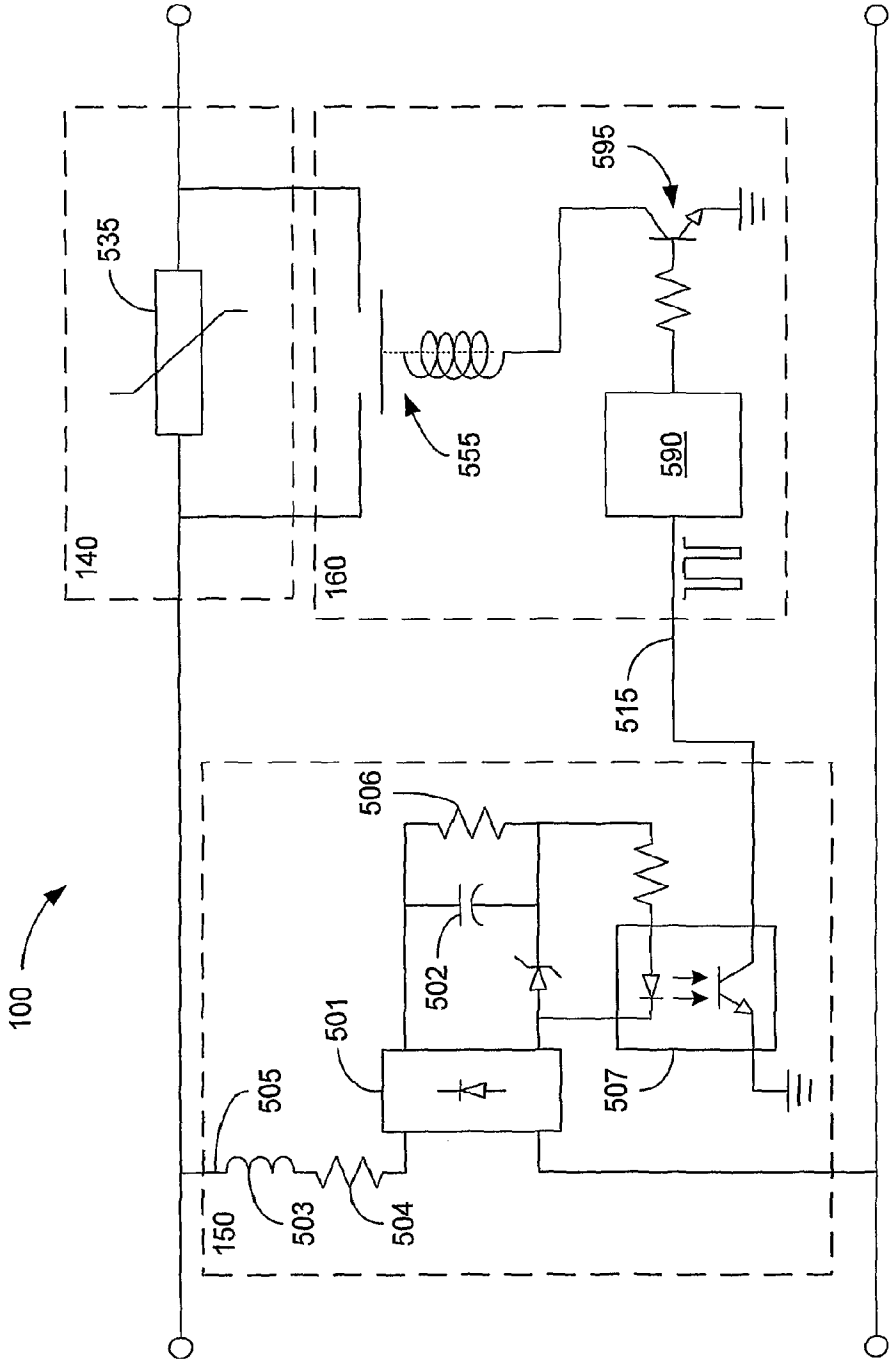

FIG. 5

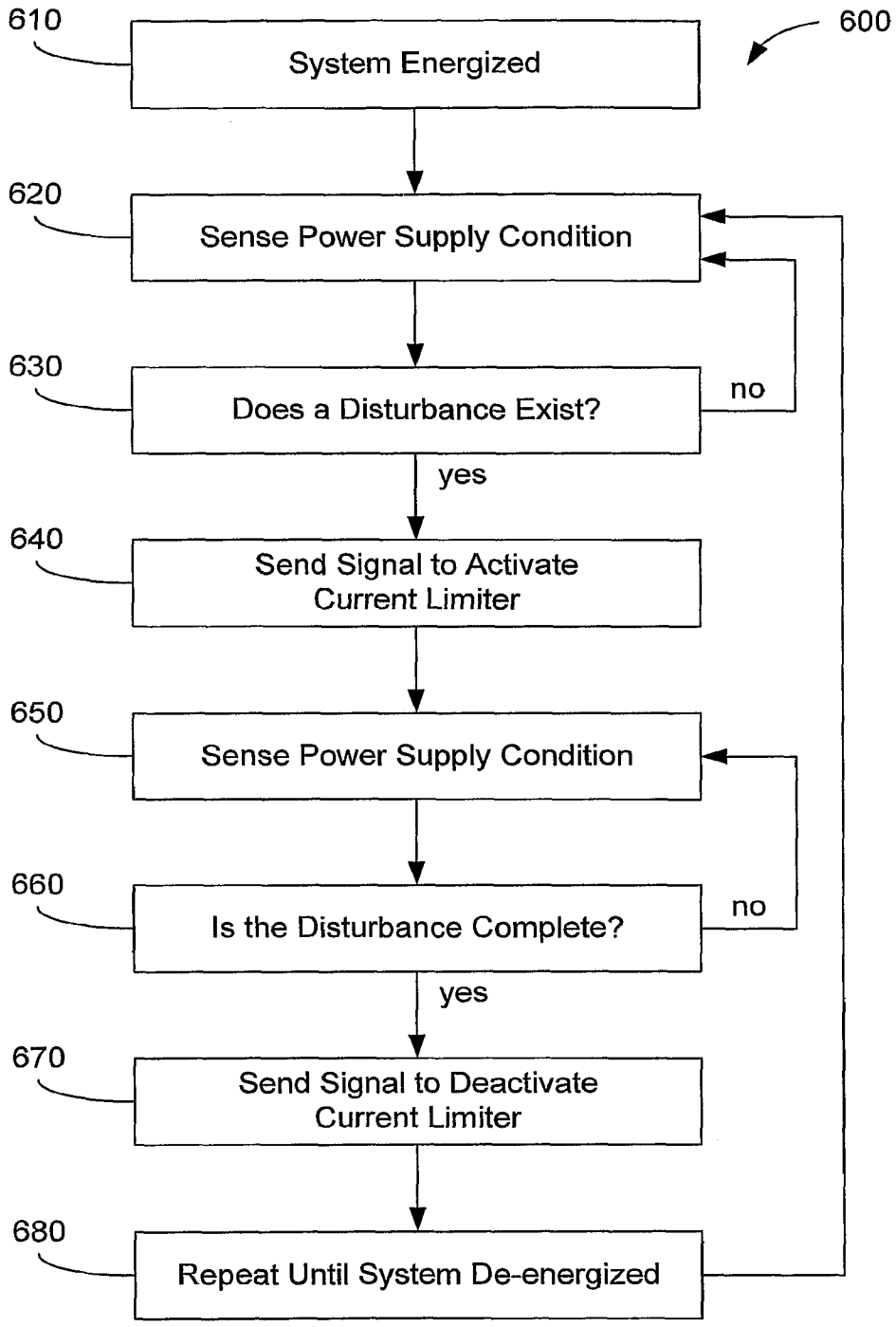
610
System Energized
600
620
Sense Power Supply Condition
630
Does a Disturbance Exist?
no
yes
640
Send Signal to Activate Current Limiter
650
Sense Power Supply Condition
660
Is the Disturbance Complete?
no
yes
670
Send Signal to Deactivate Current Limiter
680
Repeat Until System De-energized

FIG. 6

ACTIVE CURRENT SURGE LIMITERS WITH DISTURBANCE SENSOR AND MULTISTAGE CURRENT LIMITING

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 11/815,041, filed Sep. 2, 2008, entitled "ACTIVE CURRENT SURGE LIMITERS," by Deepakraj Divan, now U.S. Pat. No. 8,035,938, which is a 35 U.S.C. 371 national stage application of and claims priority to international application No. PCT/US2005/038471, filed Oct. 24, 2005, and also claims the benefit pursuant to §119(e) of and priority to U.S. Provisional Patent Application No. 60/648,466, filed on Jan. 31, 2005, entitled "System and Method for Determining Power System Transmission Line Information", the disclosures of which are incorporated herein by reference in their entireties.

This application is also related to and incorporates herein by reference each of the following patent applications:

U.S. patent application Ser. No. 13/230,251, filed Sep. 12, 2011, entitled "ACTIVE CURRENT SURGE LIMITERS WITH VOLTAGE DETECTOR AND RELAY."

U.S. patent application Ser. No. 13/230,319, filed Sep. 12, 2011, entitled "ACTIVE CURRENT SURGE LIMITERS WITH WATCHDOG CIRCUIT."

U.S. patent application Ser. No. 13/230,346, filed Sep. 12, 2011, entitled "ACTIVE CURRENT SURGE LIMITERS WITH INRUSH CURRENT ANTICIPATION."

TECHNICAL FIELD

The present disclosure is generally related to limiting current surge and, more particularly, embodiments of the present disclosure are related to actively limiting surge current produced by power supply disturbances during load operation.

BACKGROUND

There are many applications where it is necessary to protect electrical equipment from power surges and high energy transients that could damage or adversely affect the operation of such equipment. Voltage surges are commonly perceived to be the most common cause for damage to electrical equipment during operation. Voltage surges, such as those produced by lightning strikes, can cause large currents to flow resulting in damage to operating equipment. Electrical equipment utilizing electronics, such as a rectifier front end, are particularly susceptible to damage. As a result, transient voltage surge suppressors (TVSS) are commonly utilized to clamp the voltage level and absorb energy associated with a transient. However, analysis strongly suggests that there is a fairly high probability that equipment will be also be damaged by current surges that occur at the end of voltage sags. Furthermore, industrial studies have indicated that voltage sags are much more likely to occur than voltage surges. While TVSS devices limit the voltage applied to equipment, they do not limit the current surge experienced by electrical equipment at the end of voltage sag transients.

High inrush currents are also commonly experienced during the starting of electrical equipment. Inrush current limiting circuits, including a negative temperature coefficient (NTC) thermistor or resistor connected between a power supply and a protected load and a bypass switch in parallel with the NTC thermistor, are often used to mitigate the current surge seen by the load during starting. A NTC thermistor is a component with a resistance that decreases as its temperature increases. During startup, the temperature of the NTC thermistor is cold and its resistance is high. As operation continues, the temperature increases and the resistance of the NTC thermistor decreases, allowing more current during normal operation. Once the equipment has completed its startup or a preset time has elapsed, the bypass switch closes to remove the resistor from between the power supply and the electrical load. The current limiter circuit remains disabled until the equipment is de-energized and the bypass switch is reopened. While the inrush current limiter circuits limit the current surge during startup, these inrush current limiter circuits do not provide protection from electrical transients during normal operation of the electrical equipment.

SUMMARY

Briefly described, embodiments of this disclosure, among others, include active current surge limiters and methods of use. One exemplary system, among others, comprises a current limiter, including an interface configured to be connected between a power supply and a load; a disturbance sensor, configured to monitor the power supply for a disturbance during operation of the load; and an activator, configured to receive a control signal from the disturbance sensor and to activate the current limiter based on the control signal.

Another exemplary system, among others, comprises means for limiting current supplied to a load from a power supply; means for sensing a disturbance on the power supply during operation of the load; and means for activating the means for limiting current to the load when a disturbance is sensed.

Methods of use are also provided. One exemplary method, among others, comprises monitoring a condition of a power supply during operation of a load connected to the power supply; determining if the condition falls outside of an acceptable limit; and activating a current limiting device when the monitored condition falls outside of acceptable limits.

Other structures, systems, methods, features, and advantages will be, or become, apparent to one with skill in the art upon examination of the following drawings and detailed description. It is intended that all such additional structures, systems, methods, features, and advantages be included within this description, be within the scope of the present disclosure, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Many aspects of the disclosure can be better understood with reference to the following drawings. The components in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the principles of the present disclosure. Moreover, in the drawings, like reference numerals designate corresponding parts throughout the several views.

FIG. **1** illustrates an active current surge limiter.

FIG. **2** is an alternative embodiment of the active current surge limiter utilizing a microcontroller and semiconductor switches.

FIG. **3** is an alternative embodiment of the active current surge limiter utilizing a microcontroller and an electromechanical relay.

FIG. **4** is an alternative embodiment of the active current surge limiter utilizing a voltage detector and an electromechanical relay.

FIG. **5** is an alternative embodiment of the active current surge limiter utilizing an optocoupler and an electromechanical relay.

FIG. **6** is a flow chart illustrating an embodiment of a fast detection algorithm for the active current surge limiter.

DETAILED DESCRIPTION

Voltage sags have been shown to occur fairly frequently in industrial settings. Studies indicate that voltage sags are 100 to 1000 times more likely to occur than voltage surges. Data and analysis strongly suggest a high probability that operating equipment can be damaged by a current surge that occurs at the end of the voltage sag. The most vulnerable point for typical equipment is the end of short-duration sags, when the inrush limiting circuits are normally disabled. The current surge can have excessively high I^2T ratings because the normal inrush limiting circuit (NTC thermistor or resistor+bypass switch) is disabled. The current surge causes damage to equipment, as well as degradation of components leading to shortened equipment life and premature equipment failure. Industrial, commercial and residential equipment that are potentially subject to the problem include, but are not limited to, PC's, servers, TV's, stereo amplifiers, microwave ovens, PLC's, robots, machine drives, medical equipment, etc.

Embodiments of active current surge limiters are described below. It should be emphasized that the described embodiments are merely possible examples of implementations, and are set forth for clear understanding of the principles of the present disclosure, and in no way limit the scope of the disclosure.

FIG. **1** illustrates an active current surge limiter. The active current surge limiter **100** is connected at an interface between a power supply **110** and a load **120**. Power supplies include AC and/or DC sources. While the principles discussed are generally applied to applications up to 1000 Volts, this does not prevent their use in applications at higher voltage levels. Loads that are sensitive to these disturbances include, but are not limited to, industrial, commercial and residential equipment that include electronic components that operate with a DC power supply. A transient voltage surge suppressor (TVSS) **130** connected on the input side can provide the added functionality of a voltage surge suppressor device. The active current surge limiter **100** includes a current limiter **140** for limiting the current supplied to the connected load **120**, a disturbance sensor **150** for monitoring the condition of the power supply **110**, and an activator **160** for activating the current limiter **140** when the disturbance sensor detects a disturbance on the power supply.

Disturbances in the power supply can include variations in the power supply characteristics such as, but are not limited to, the voltage, current, and combinations thereof. The presence of a power supply disturbance is indicated when the sensed characteristic falls outside established operational limits. Operational limits can be preset based on variables such as, but not limited to, industrial standards and known load and supply characteristics. However, as the power supply and load characteristics are typically unknown, establishment of allowable current limits can require additional analysis. Another alternative is to allow the disturbance sensor **150** to establish limits based on continuous monitoring of selected supply characteristics.

FIG. **2** is an alternative embodiment of the active current surge limiter utilizing a microcontroller and power semiconductor switches. This non-limiting embodiment of an active current surge limiter **100**, the disturbance sensor **150** uses a microprocessor or microcontroller **200** to establish allowable current limits, continuously monitor power supply characteristics (i.e. sensing voltage **205** and current **210**), and communicate a control signal **215** to the activator **160** indicating the presence of a disturbance on the power supply. The described control strategy allows the active current surge limiter **100** to handle power-up and load change without problems.

To establish the allowable current limit, the circuit in FIG. **2** senses and measures the current **210** drawn by the load **120**, including peak current at start-up, through a current transformer **220**. The peak current at start-up is stored in a peak-rectifier circuit (not shown), including a diode and capacitor coupled with a current transformer, and measured by an A/D converter incorporated in the microcontroller **200**. One skilled in the art would realize that other measurement circuits could also be utilized to measure power supply characteristics. The starting current is recorded and stored by the microcontroller **200** as a peak inrush current. During operation of the load **120**, the microcontroller **200** continues to monitor the load current **210** and record any sensed peak currents.

The microcontroller **200** also monitors the incoming ac line voltage **205**. Limits for the sensed voltage **205** can be preset or established by the microcontroller **200**. Voltage sags occur when a supply voltage drops below a predetermined level, such as but not limited to, 90% of rated voltage for short periods of time of one half cycle or more. When a sag in the monitored line voltage **205** is detected by the microcontroller **200**, a peak current limit reference (I_{max}) is set to the maximum peak current value thus far recorded. During a voltage sag or momentary interruption, the current drawn by the load is most likely to decrease. At the end of the voltage sag, the voltage can quickly return to normal, causing a surge in the sensed current **210**. The magnitude of the surge current is affected by load factors, such as the type, condition, and proximity as well as power supply factors, such as magnitude and duration of disturbance, line impedance, return profile of the line voltage, and transformer location. Industrial, commercial and residential equipment vulnerable to the effects of current surges include, but not limited to, PC's, servers, TV's, stereo amplifiers, microwave ovens, PLC's, robots, machine drives, and medical equipment. Moreover, any equipment utilizing rectifier/capacitor circuits amplify the surge current effects when the capacitor is substantially discharged during a voltage sag.

Once the microcontroller **200** detects a current level that exceeds the I_{max} threshold, a control signal **215** is sent to the activator **160** indicating the presence of a disturbance. In this non-limiting embodiment, the current limiter **140** is activated by turning off a semiconductor switch **225** through a gate drive **230**. Activation of the current limiter **140** forces the load current to flow through an ac voltage clamping device **235**, such as but not limited to, a varistor. The voltage impressed across the load **120** is reduced, limiting the current supplied to the load. The switch **225** can then be turned on at, but not limited to, the next cycle, a zero crossing point, and a predetermined number of switching under a high frequency duty cycle control scheme as is customary in PWM circuits. If the sensed current **210** remains high for greater than a preset period of time, such as but not limited to one to two seconds, then a trip signal **240** is activated by the microcontroller **200**, opening an overload switch or circuit breaker **245** and shutting the system down until a reset is effectuated, e.g., a reset button is pressed. Incorporation of a voltage clamping device **250** provides additional voltage surge protection to the connected load **120**.

The use of gate turn-off devices **225** allows turn-off and over-current protection even under normal voltage conditions

as well as in the presence of fast rising current fronts that occur under fault conditions. For successful operation, the components are sized to handle trapped energy in line and load inductances. In addition, power dissipation during continuous operation should be considered during selection.

FIG. **3** is an alternative embodiment of the active current surge limiter utilizing a microcontroller and an electromechanical relay. This non-limiting embodiment utilizes the same disturbance sensor **150** to sense voltage **205** and current **210** as depicted in FIG. **2**. During normal operation, the current limiter **140** can be bypassed using an electromechanical relay, contactor or switch. In this depiction, a control signal **215** sent by the microcontroller **200** causes a normally open relay **355** to close and deactivate the current limiter **140**. The power supply is continuously monitored as described for FIG. **2**.

Fast detection algorithms (e.g., as described in FIG. **6**) allow the detection of supply disturbances within one quarter to one half cycle. Fast detection algorithms can be implemented in, but not limited to, software, hardware and/or individual components. Because the line current drawn by the load typically drops dramatically when the DC capacitor reverse biases the diode bridge during a voltage sag, a voltage sag that is likely to cause inrush current can be can readily detected. Upon detecting the onset of the voltage sag, the control signal **215** causes the relay **355** to open and activating the current limiter **140**.

The current limiter **140** in this embodiment includes two resistors, **360** and **365**, with a thyristor pair or triac **370** connected in parallel with the second resistor **365**. Alternative combinations can also be utilized. Upon exceeding I_{max}, resistors **360** and **365** provide a high resistance to limit current to the attached load. After a sufficient time delay or a determination that the sensed current **210** is below an allowable level, the triac **370** is turned on, allowing higher current levels. Control of the triac **370** is provided by a signal **375** sent by the microcontroller **200** to a gate driver **330** for the triac **370**. Once the sensed current **210** subsides or after sufficient time has elapsed, the relay **355** is reclosed allowing normal load operation to resume. As described for FIG. **2**, if the sensed current **210** remains high for a predetermined period, a trip signal **240** is activated by the microcontroller **200**, opening an overload switch or circuit breaker **245** and shutting the system down.

With the use of a multi-step current limiter **140**, it is possible to significantly improve the performance so as to minimize impact on the load. The level of surge current that flows in the system depends on a number of parameters including, but not limited to, the depth and duration of the voltage sag, the load rating, the short circuit current available at the load point, and the amount of capacitance in the load rectifier. Monitoring of I_{max} provides an indication of the load characteristics and maximum current necessary for normal operation. The current flowing through the resistors **360** and **365** forward biases the diode and provides an indication of the effective DC bus voltage (V_{dc}) in the load. If triac **370** is turned on at an angle α, the difference between the line and DC bus voltages ($V_{line}-V_{dc}$) is applied across resistor **360** and allowing an increase in current flow to the load **120**. Neglecting line and load inductances, the line current decreases until, at an angle β, it reaches to zero when the line voltage equals V_{dc}. By controlling the turn-on of triac **370**, it is possible to control the average current supplied to the load capacitance and minimize recovery time. As V_{dc} increases with capacitor charging, α automatically changes to keep the line current limited and under control. Once the current drawn by load has returned to within allowable limits, the relay **355** can be closed again, allowing normal operation to resume.

This approach allows us to match the allowed inrush current to the load characteristic, as represented by I_{max}, and the average current drawn by the load, without requiring the use of gate turn-off devices **225**. In addition, the use of triacs **370** simplifies the gating and control requirements, reducing cost and complexity. Furthermore, as the triac **370** and the resistors **360** and **365** are normally deactivated by relay **355** and only operate during transients, the power dissipation requirements are minimal, allowing packaging in a more compact form. Other combinations of resistors and switching elements, such as but not limited to triacs, can be used to control current flow.

This embodiment can also provide a soft start process for equipment without built-in startup protection. Upon power-up, a two-stage soft start process is initiated. First, resistors **360** and **365** provide a high resistance to limit inrush current. After sensed current **210** subsides to an allowable level or a preset time, triac **370** is turned on to allow higher current levels. Finally, once the current level again subsides or sufficient time has elapsed, the relay **355** is closed allowing normal load operation to begin.

FIG. **4** is an alternative embodiment of the active current surge limiter utilizing a voltage detector and an electromechanical relay. In this non-limiting embodiment, a normally open relay **455** is used to activate the current limiter **140**, which includes a resistor or Negative Temperature Coefficient (NTC) thermistor **435**. The NTC thermistor **435** has a high resistance value when cold. The resistance drops dramatically as the NTC thermistor **435** heat up, often by a factor of 10 or more, allowing higher currents to flow. The high resistance returns as the NTC thermistor **435** cools off. Manufacturers typically specify cooling times of up to 60 seconds or more.

At startup, the relay **455** is maintained off (open) and the NTC thermistor **435** limits the inrush current that flows. As current flows, the resistance of the NTC thermistor **435** decreases providing less current limitation. After a preset time delay, the relay **455** is turned on to de-energize the current limiter **140** by bypassing the NTC thermistor **435**. This allows the NTC thermistor **435** to cool down and restore the high resistance mode.

A detector circuit **400** is implemented that identifies when a voltage sag occurs, and send a control signal **415** to activate the current limiter **140**. One of many possible implementations of the detector circuit **400** utilizes a microprocessor with an A/D converter to sense and measure the line voltage **405**. The microprocessor identifies when the voltage falls outside a nominally acceptable boundary defined by a preset limit. When a disturbance is detected, the detector circuit **400** sends a control signal **415** to a timer circuit **480**, which causes the relay **455** to open and activate the current limiter **140**. As described above, the resistance of the NTC thermistor **435** limits the surge current until the voltage is seen to return to normal conditions. After this, the NTC thermistor **435** can be bypassed after a preset time. At that point, the timer circuit **480** de-energizes the relay **455** bypassing the NTC thermistor **435**. Incorporation of a voltage clamping device **450** provides additional voltage surge protection to both the connected load **120** and the active current surge limiter **100**.

FIG. **5** is an alternative embodiment of the active current surge limiter utilizing an optocoupler and an electromechanical relay. This non-limiting embodiment uses a circuit for simulating the operation of a DC power supply in the disturbance sensor. The diode bridge **501** and the capacitor **502** represent a typical rectifier/capacitor circuit that may be used

in a load **120**. The inductance **503** and resistance **504** simulate effective line impedance. The time constant of the load resistor **506** and capacitor **502** is chosen to be similar to that found in rectifier/capacitor circuits. This circuit simulates the operation of a high power rectifier/capacitor circuit at low cost. The capacitor **502** is charged from the line at the peaks of the sensed line voltage **505**, as the simulated load would. An optocoupler **507** is used to detect the charging current pulse at the line voltage peaks and send a control signal **515** to the activator **160**.

A retriggerable monostable multi-vibrator **590** with an output pulse greater than one half cycle (8.33 mS) is triggered by the control signal **515** from the optocoupler **507**. As long as the charging current pulses occur every half cycle, the monostable multi-vibrator **590** remains triggered. The output of the monostable multi-vibrator **590** is used to close the relay **555** through a semiconductor switch **595**, such as but not limited to, a transistor. While the line voltage is within specified limits, the relay **555** is maintained closed, de-energizing the current limiter **140** by bypassing a current limiting device **535**, such as but not limited to, an NTC thermistor, triac, and resistor. It should be clear to one skilled in the art that the timing and control functions could be performed by a microprocessor or microcontroller. This implementation allows for current surge limiting without a current sensor.

If the sensed voltage **505** decreases in amplitude below the simulated DC bus voltage, the charging current pulses stop, causing the optocoupler **507** to stop sending triggering pulses as the control signal **515**. When the triggering pulses stop, the monostable multi-vibrator **590** output changes state at the end of the timing period, causing switch **595** to turn the relay off after a selectable delay. This then reinserts the current limiting device **535** into the circuit. When the voltage returns to normal, the current limiting device **535** limits the inrush current to the load **120**. When the AC line voltage returns to normal, the charging current pulses begin again and the monostable multi-vibrator **590** is retriggered once again. After waiting for a preset time, the relay **555** is closed once again, de-energizing or bypassing the current limiter **140**.

FIG. **6** is a flow chart illustrating an embodiment of a fast detection algorithm **600** for the active current surge limiter. Fast detection algorithms **600** can be implemented in, but not limited to, software, hardware and/or individual components, as illustrated in the previous embodiments of FIGS. **2-5**. In this non-limiting embodiment of a fast detection algorithm **600**, the active current surge limiter **100** is energized (**610**) upon starting the connected load **120**. The active current surge limiter **100** begins sensing the power supply conditions (**620**). This can include, but is not limited to, voltage, current, and combinations thereof. The sensed conditions are then evaluated to determine if a disturbance exists (**630**). If it is determined that no disturbance exists, then the active current surge limiter **100** continues to sense (**620**) and evaluate (**630**) the power supply condition. If a disturbance does exist, then the current limiter **140** is activated (**640**).

Once the current limiter **140** is activated, the active current surge limiter **100** returns sensing the power supply conditions (**650**). The sensed conditions are then evaluated to determine if the disturbance is complete (**660**). If it is determined that the disturbance still exists, then the active current surge limiter **100** continues to sense (**650**) and evaluate (**660**) the power supply condition. If the disturbance no longer exists, then the current limiter **140** is deactivated (**670**). The process repeats until the active current surge limiter **100** and its load **120** are de-energized. Appropriate time delays, as discussed above, can be incorporated to optimize system operation and protection.

It should be emphasized that the above-described embodiments of the present disclosure are merely possible examples of implementations, and are merely set forth for a clear understanding of the principles of the disclosure. Many variations and modifications may be made to the above-described embodiments for use in single or multi-phase systems. For example, a plurality of devices can be included in the current limiter to provide active of passive current limitation. In addition, a plurality of circuits utilizing integrated circuits or discrete components can be implemented to provide disturbance sensing and activation of the current limiter. Moreover, other automated methods to determine voltage and current limitations can be incorporated into active current surge limiters. All such modifications and variations are intended to be included herein within the scope of this disclosure and protected by the following claims.

Therefore, at least the following is claimed:

1. A method for reducing inrush current to an electrical load in response to detection of a disturbance occurring in an input AC power supply coupled to the electrical load, comprising:

applying an input voltage to the electrical load;

monitoring the current drawn by the load;

recording peak values of the current drawn by the load;

continuously monitoring the voltage of the input AC power supply to detect a voltage sag to a predetermined level below rated voltage for short periods of time of one half cycle or more indicating a disturbance in the input AC power supply that would cause an inrush current to the electrical load upon ending of the disturbance;

in response to detection of the voltage sag, recording a peak current limit reference (I_{max}) corresponding to a maximum peak current value thus far recorded;

detecting when the current level exceeds the peak current limit reference (I_{max}) as indicating the disturbance occurring in the input AC power supply; and

adding an impedance to the electrical load in response to detecting the disturbance, wherein an inrush current to the electrical load is limited as the input voltage returns to a normal operating level voltage.

2. The method of claim **1**, wherein the disturbance is sustained for a duration until the input voltage has returned to a normal operating level voltage, and further comprising the step of removing the impedance from the electrical load after the input voltage has returned to a normal operating level voltage.

3. The method of claim **1**, further comprising removing the impedance when the input voltage returns to normal operating level voltage.

4. The method of claim **1**, further comprising removing the impedance after a predetermined duration.

5. The method of claim **1**, further comprising removing the electrical load when the inrush current exceeds a predetermined value for a predetermined duration.

6. The method of claim **1**, further comprising the steps of:

establishing an allowable current limit for the electrical load by sensing and measuring the current drawn by the load at start-up; and

adding the impedance to the electrical load in response to a determination that the inrush current would exceed the allowable current limit upon ending of the disturbance.

7. The method of claim **6**, wherein the allowable current limit for the electrical load is established by sensing and monitoring the current drawn by the load at startup, and storing the peak current at start-up as the allowable current limit.

8. The method of claim 6, wherein the allowable current limit at start-up is detected and stored by a peak-rectifier circuit.

9. The method of claim 6, wherein the allowable current limit is measured by an A/D converter associated with a microcontroller that effects the continuous monitoring.

10. The method of claim 9, wherein the starting current representing the allowable current limit is recorded and stored by the microcontroller as a peak inrush current.

11. The method of claim 1, wherein the disturbance comprises a voltage sag below about 90% of rated voltage for a period of time one half cycle or more.

12. The method of claim 1, wherein the step of continuous monitoring of predetermined characteristics of the input AC power supply is effected by a programmed microcomputer.

13. The method of claim 1, wherein the predetermined characteristics of the input AC power supply comprises the voltage, the current, or a combination of both.

14. The method of claim 1, further comprising the step of activating a circuit breaker configured to de-energize the electrical load when an inrush current to the electrical load exceeds a predetermined value for a predetermined duration.

15. The method of claim 1, wherein the monitoring of current drawn by the load is via a current transformer coupled to the input AC power supply and coupled to an A/D converter associated with a programmed microcontroller.

16. The method of claim 1, wherein the monitoring of the voltage of the input AC power supply and detecting the voltage sag is via an A/D converter coupled to a programmed microcontroller.

17. The method of claim 1, further comprising the step of measuring the starting current drawn by the load at start-up.

18. The method of claim 17, further comprising the step of recording and storing the starting current as a peak current value.

19. The method of claim 1, wherein a voltage sag comprises a voltage level of 90% of rated voltage.

20. The method of claim 1, wherein the impedance is a negative temperature coefficient (NTC) resistor.

21. The method of claim 1, wherein the impedance comprises a resistor and a triac.

22. A system for reducing inrush current to an electrical load in response to detection of a disturbance occurring on an input AC power supply coupled to the electrical load, comprising:

a control circuit including a programmed microcontroller configured to detect a disturbance in the input AC power supply during steady-state operation of an electrical load by continuously monitoring the voltage of the input AC power supply and the current drawn by the load and provide a control signal;

a current limiting device configured to be selectively connected between the input AC power supply and the electrical load;

an activator configured to receive the control signal from the control circuit and to insert the current limiting device based on the control signal;

wherein the microcontroller is programmed to record peak values of the current drawn by the load;

wherein the microcontroller is programmed to detect a voltage sag in the input AC power supply to a predetermined level below rated voltage for short periods of time of one half cycle or more indicating a disturbance in the input AC power supply that would cause an inrush current to the electrical load upon ending of the disturbance;

wherein the microcontroller is programmed, in response to detection of the voltage sag, to record a peak current limit reference (I_{max}) corresponding to a maximum peak current value thus far recorded; and

wherein the microcontroller is programmed to detect when the current level exceeds the peak current limit reference (I_{max}) as indicating the disturbance occurring in the input AC power supply and to provide the control signal to the activator to insert the current limiting device.

23. The system in claim 22, further comprising a circuit breaker configured to de-energize the electrical load when an inrush current to the electrical load exceeds a predetermined value for a predetermined duration.

24. The system in claim 22, wherein the disturbance is sustained for a duration until the input voltage has returned to a normal operating level voltage, and further comprising the step of removing the impedance from the electrical load after the input voltage has returned to a normal operating level voltage.

25. The system in claim 22, wherein the control circuit comprises a simulated power supply comprising a rectifier, a capacitor and a source impedance.

26. The system in claim 22, wherein the control circuit is a solid-state device.

27. The system in claim 22, wherein the current limiting device is a negative temperature coefficient (NTC) resistor.

28. The system in claim 22, wherein the current limiting device comprises a resistor and a triac.

29. The system in claim 22, further comprising a circuit for establishing an allowable current limit for the electrical load by sensing and measuring the current drawn by the load at start-up; and

wherein the control circuit is operative to add the current limiting device to the electrical load in response to a determination that the inrush current would exceed the allowable current limit upon ending of the disturbance.

30. The system in claim 29, wherein the allowable current limit for the electrical load is established by sensing and monitoring the current drawn by the load at startup, and storing the peak current at start-up as the allowable current limit.

31. The system in claim 29, further comprising a peak-rectifier circuit for detecting and storing the allowable current limit at start-up.

32. The system in claim 29, further comprising an A/D converter associated with a microcontroller that effects the continuous monitoring and sensing and measuring the allowable current limit.

33. The system in claim 32, wherein the starting current representing the allowable current limit is recorded and stored by the microcontroller as a peak inrush current.

34. The system in claim 22, wherein the disturbance comprises a voltage sag below about 90% of rated voltage for a period of time one half cycle or more.

35. The system in claim 22, wherein the predetermined characteristics of the input AC power supply comprises the voltage, the current, or a combination of both.

36. The system in claim 22, further comprising a circuit breaker configured to de-energize the electrical load when an inrush current to the electrical load exceeds a predetermined value for a predetermined duration as determined by the control circuit.

37. The system of claim 22, wherein the monitoring of current drawn by the load is via a current transformer coupled to the input AC power supply and coupled to an A/D converter associated with the programmed microcontroller.

38. The system of claim 22, wherein the monitoring of the voltage of the input AC power supply and detecting the voltage sag is via an A/D converter coupled to the programmed microcontroller.

39. The system of claim 22, wherein the microcontroller is programmed to measure the starting current drawn by the load at start-up.

40. The system of claim 39, wherein the microcontroller is programmed to record and store the starting current as a peak current value.

41. A multi-step active current surge limiting apparatus for reduction of inrush current to an electrical load in response to detection of a disturbance in an input AC power supply coupled to the electrical load, comprising:

a current-limiting circuit coupled between the input power supply and the electrical load, the current-limiting circuit comprising:

(a) a current limiting impedance comprising (i) first resistor, (ii) a second resistor in series with the first resistor, and (iii) a switch in parallel with the second resistor that is actuated by a first control signal to bypass the second resistor, and

(b) a relay in parallel with the current limiting impedance and having contacts that are in an open position to couple the input AC power supply to the electrical load through the current limiting impedance and close in response to a second control signal to couple the input AC power supply to the electrical load and bypass the current limiting impedance; and

a control circuit that provides the first control signal and the second control signal to provide multiple levels of impedance to the inrush of current to the electrical load in response to predetermined conditions.

42. The apparatus of claim 41, wherein the control circuit comprises a programmed microprocessor connected to receive signals representing the voltage of the input power supply provided from an analog-to-digital (A/D) converter, the microprocessor programmed to identify when the voltage falls outside a nominally acceptable boundary defined by a preset limit, and to provide the first control signal and the second control signal.

43. The apparatus of claim 41, wherein the control circuit comprises a programmed microprocessor connected to receive signals representing the voltage of the input power supply provided from an analog-to-digital (A/D) converter, the microprocessor providing the first control signal to cause the relay to open and then close after a predetermined time after the voltage returns to a normal level.

44. The apparatus of claim 41, wherein the disturbance in the input power supply is a voltage disturbance, a current disturbance, or a combination thereof.

45. The apparatus of claim 41, wherein the switch is a semiconductor switch.

46. The apparatus of claim 45, wherein the semiconductor switch is selected from the group comprising a thyristor and a triac.

47. The apparatus of claim 41, wherein the switch is in the open position and the relay is in the open position at start-up so that the first resistor and the second resistor provide maximum impedance.

48. The apparatus of claim 41, wherein the switch is in the closed position and the relay is in the open position so that only the first resistor provides a current limiting impedance.

49. The apparatus of claim 41, wherein after a start-up condition where the switch and the relay are open so that the first resistor and the second resistor provide a current limiting impedance, the control circuit closes the switch to allow a greater current to flow and thereafter closes the relay to bypass the current-limiting circuit.

50. The apparatus of claim 41, further comprising a selectively actuatable circuit breaker coupled prior to the current-limiting circuit that is responsive to a trip signal to provide further protection for the load and for the apparatus if the sensed current remains excessive for a predetermined period.

51. The apparatus of claim 41, wherein the control circuit is operative to turn on the switch at a predetermined first phase angle (α) in the cycle of the input AC power supply so as to allow additional current to flow to the load, and is operative to turn off the switch as a predetermined second phase angle (β) in the cycle of the input AC power supply.

52. The apparatus of claim 51, wherein the predetermined first phase angle (α) in the cycle of the input AC power supply is determined when the line voltage V_{line} exceeds the effective DC bus voltage V_{dc} at the load.

53. The apparatus of claim 52, wherein the predetermined second phase angle (β) in the cycle of the input AC power supply is determined when the line voltage V_{line} is about equal to the effective DC bus voltage V_{dc} at the load.

54. The apparatus of claim 41, wherein the switch is controlled by the control circuit so as to control the average current applied to the load capacitance and minimize recovery time.

55. The apparatus of claim 51, wherein the predetermined first phase angle (α) in the cycle of the input AC power supply is automatically changed by the control circuit to maintain limited line current as a function of capacitor charging.

56. The apparatus of claim 41, wherein the resistors in the current-limiting circuit only operate during transients.

57. The apparatus of claim 41, wherein the apparatus provides a soft start process for equipment without built-in start-up protection, by (a) initially coupling the first resistor and the second resistor to the equipment at startup, (b) sensing the inrush current with a current sensor, (c) turning on the switch when the current is at an allowable level or after a preset time period to allow additional current to flow, and (d) closing the relay after the current level again subsides or after a second preset time period.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 8,582,262 B2
APPLICATION NO. : 13/230190
DATED : November 12, 2013
INVENTOR(S) : Deepakraj Malhar Divan

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page, item [63] Related U.S. Application Data should read as follows:

"Continuation of application No. 11/815,041, filed on Sep. 2, 2008, now Pat. No. 8,035,938, which is a 371 of application No. PCT/US2005/038471, filed on Oct. 24, 2005."

Signed and Sealed this
Sixth Day of May, 2014

Michelle K. Lee

Michelle K. Lee
Deputy Director of the United States Patent and Trademark Office